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Erdös number: 3, **H-index:** 28 (Harzing's PoP), 2 best paper awards.

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[**W9**] P. Engelke, I. Polian, M. Renovell, B. Seshadri, and B. Becker. The pros and cons of very-low-voltage testing: an analytical view. In *GI/ITG Workshop "Testmethoden und Zuverlässigkeit von Schaltungen und Systemen"*, pages 149–153, Dresden, D, 2004.

[**W8**] I. Polian and B. Becker. Reducing ATE cost in system-on-chip test. In *IEEE Int'l Workshop on Test Resource Partitioning*, Napa Valley, CA, USA, 2003.

[**W7**] P. Engelke, I. Polian, M. Renovell, and B. Becker. Simulating resistive bridging and stuck-at faults. In *IEEE Int'l Workshop on Current and Defect-Based Testing*, pages 49–56, Napa Valley, CA, USA, 2003.

[**W6**] I. Polian, W. Günther, and B. Becker. The case for 2-POF. In *ITG/GI/GMM-Workshop "Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen"*, Bremen, D, 2003.

[**W5**] I. Polian, and B. Becker. Optimal bandwidth allocation in concurrent SoC test under pin number constraints. In *IEEE Workshop on RTL ATPG and DfT*, Guam, USA, 2002.

[**W4**] I. Polian, I. Pomeranz, and B. Becker. Exact computation of maximally dominating faults and its application to n-detection tests. In *IEEE European Test Workshop*, Korfu, GR, 2002. (poster)

[**W3**] J. Bradford, H. Delong, I. Polian, and B. Becker. Realistic fault simulation in an industrial setting. In *GI/ITG Workshop "Testmethoden und Zuverlässigkeit von Schaltungen und Systemen"*, Bad Herrenalb, D, 2002.

[**W2**] I. Polian and B. Becker. Multiple scan chain design for two-pattern testing. In *IEEE Latin American Test Workshop*, pages 156–161, Cancun, MX, 2001.

[**W1**] I. Polian, W. Günther, and B. Becker. Efficient pattern-based verification of connections to intellectual property cores. In *ITG/GI/GMM-Workshop "Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen"*, pages I:111–120, Meissen, D, 2001.

Tutorials, Panels, Special Sessions

[**T24**] "Security of emerging architectures". Special Session co-organizer. *Int'l Conf. on CAD*, San Diego, CA, USA, 2018.

[**T23**] "Funding hardware security research: Taxpayer's money to support malicious hackers?" Panel organizer. *Int'l Verification and Security Workshop*, Platja d'Aro, ES, 2018.

[**T22**] "Controlled fault injection: wishful thinking, thoughtful engineering, or just luck?" Panelist. *Workshop on Fault Diagnosis and Tolerance in Cryptography*, Taipeh, TW, 2017.

[**T21**] "Secure multi-processors systems-on-chip for critical applications." Special Session co-organizer. *IEEE Conf. on System-on-Chip Design*, Munich, D, 2017.

[**T20**] "DFT vs. security – Is it a contradiction? How can we get the best of both worlds?" Panelist. *IEEE Int'l Verification and Security Workshop*, Sant Feliu de Guixols, ES, 2016.

[**T19**] "Test of secure devices". *TRUDEVICE Training School on Trustworthy Manufacturing and Utilization of Secure Devices*, Leukerbad, CH, 2016.

[**T18**] "Emerging probabilistic circuits from stochastic to quantum: Will they scale?" Special Session organizer. *ACM/IEEE Design Automation Conf.*, San Francsco, CA, USA, 2015.

[**T17**] "Counterfeit IC identification: How can test help?" Hot topic organizer. *IEEE VLSI Test Symp.*, Berkeley, CA, USA, 2013.

[**T16**] "Current testing: Dear or alive?" Panelist. *IEEE European Test Symp.*, Avignon, F, 2013.

[**T15**] "Fault-based attacks on cryptographic hardware." Embedded tutorial presenter. *IEEE Int'l Symp. on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, Karlowy Vary, CZ, 2013.

[**T14**] "Quantum Informatics: Classical circuit synthesis, resource optimisation and benchmarking." Special session organizer. *IEEE Asian Test Symp.*, Niigata, J, 2012.

[**T13**] "Cross-layer reliability." Special topic organizer. *Int'l Workshop on Impact of Low-Power Design on Test and Reliability*, Annecy, FR, 2012.

[**T12**] "Adaptive techniques for energy-reliability trade-offs." Special topic organizer. *Int'l Workshop on Impact of Low-Power Design on Test and Reliability*, Trondheim, NO, 2011.

[**T11**] "Volume diagnosis: Power in numbers?" Panel organizer and moderator. *IEEE Workshop on Reliability-Aware System Design and Test*, Chennai, IN, 2011.

[**T10**] "Testing nanoelectronic circuits under massive statistical process variations." Special session organizer. *IEEE Asian Test Symp.*, Shanghai, CN, 2010.

[**T9**] "Massive statistical process variations: A grand challenge for testing nanoelectronic circuits." Special session organizer. *Intl Workshop on Dependable and Secure Nanocomputing*, Chicago, IL, USA, 2010.

[**T8**] "Searching high and low for the right test." Special session organizer. *Int'l Workshop on Impact of Low-Power Design on Test and Reliability*, Prague, CZ, 2010.

[**T7**] "Low-power test and noise-aware test: Foes or friends?" Panel organizer. *IEEE VLSI Test Symp.*, Santa Cruz, CA, USA, 2010.

[**T6**] "End of CMOS roadmap – reliability and test challenges." Panel organizer and moderator. *IEEE Workshop on Reliability-Aware System Design and Test*, Bangalore, IN, 2010.

[**T5**] "Test of power supply noise – causes, effects and testing." Tutorial presenter. *Int'l Workshop on Impact of Low-Power Design on Test and Reliability*, Sevilla, E, 2009.

[**T4**] "Benchmarking academic DFT tools on the OpenSparc microprocessor." Panelist. *Int'l Test Conf.*, Santa Clara, CA, USA, 2008.

[**T3**] "Defect-tolerance, error-tolerance: which way to go? How?" Panelist. *IEEE Workshop on RTL ATPG and DfT*, Beijing, CN, 2007.

[**T2**] "Error-tolerance: Are good-enough chips good-enough?" Panel organizer and moderator. *IEEE European Test Symp.*, Freiburg, D, 2007.

[**T1**] "Soft errors in micro and nanoelectronics." Embedded tutorial presenter. *GMM/GI/ITG Reliability and Design Conf.*, Munich, D, 2007.

Invited Presentations (Not refereed)

1. "Hardware security and test: Friends or enemies?" Keynote at the International Symposium on Dependable Integrated Systems, Fukuoka, November 2016.

2. "Hardware Trojans: An emerging threat for the Internet of Things". Universita della Svizzera Italiana, Lugano, October 2016 (Host: Dr. Francesco Regazzoni).

3. "Hardware Trojans: An emerging threat for the Internet of Things". EPFL Summer Research Institute, Lausanne, June 2016 (Host: Prof. Brian Ford).

4. "Hardware Trojans in early design steps: An emerging threat". Dagstuhl Seminar "Hardware Security", May 2016.

5. "Paradigm shifts in Electronics". FRIAS lectures series "Paradigm Shifts in Science", Freiburg Institute of Advanced Studies, May 2016 (Host: Prof. Bernd Kortmann).

6. "Parametric Trojans for fault-based attacks on cryptographic hardware". RSS Management Committee Meeting, October 2015 (Host: Prof. Ulf Schlichtmann).

7. "Parametric Trojans for fault-based attacks on cryptographic hardware". Bar-Ilan University, Ramat Gan, Israel, April 2015 (Host: Dr. Osnat Keren).

8. "Parametric Trojans for fault-based attacks on cryptographic hardware". University of Massachusetts, Amherst, USA, April 2014 (Hosts: Prof. Sandip Kundu, Prof. Israel Kundu and Prof. Wayne Burleson).

9. "Implications of extreme variability on architecture and test". Dagstuhl NSF/SRC/DFG Joint Workshop "Bugs and Defects in Electronic Systems: The Next Frontier", April 2013.

10. "Towards scalable quantum computing: Algorithmic challenges", National Institute of Informatics, Tokyo, Japan, March 2013 (Hosts: Prof. Kae Nemoto and Prof. Simon Devitt).

11. "Towards a cross-layer strategy against fault-based attacks'. Dagstuhl seminar "Verifying Reliability", August 2012.

12. "Advanced test generation techniques for non-standard fault models". Kyushu Institute of Technology, Iizuka, Japan, February 2012 (Host: Prof. Xiaoqing Wen).

13. "Advanced test generation techniques for non-standard fault models". Synopsys Inc., Mountain View, USA, September 2011 (Host: Dr. Alodeep Sanyal).

14. "Energy-reliability trade-offs in nanoscale electronics". University of Frankfurt, Germany, June 2011 (Host: Prof. Isolde Adler).

15. "Adaptive voltage over-scaling for resilient applications". University of Michigan, Ann Arbor, USA, June 2010 (Host: Prof. John P. Hayes).

16. "Test and reliability of nanoscale electronic systems: next-generation solutions for next-generation challenges". University of Southern California, Los Angeles, USA, October 2008 (Host: Prof. Dr. Sandeep Gupta).

17. "Test, verfication and validation of products". Endress & Hauser Flowtec, Reinach, Switzerland, May 2007 (Host: Dr. Ulrich Kaiser).

18. "Resource-constrained error handling in digital circuits". Intel Santa Clara, USA, May 2007 (Host: Dr. Abhijit Jas).

19. "Transient-error tolerance". South European Test Seminar, Sestriere, Italy, March 2006.

20. "Transient-error tolerance". Nara Institute of Science and Technology (NAIST), Nara, Japan, November 2006 (Host: Prof. Hideo Fujiwara).

21. "Transient-error tolerance". Yale University, New Haven, USA, October 2006 (Host: Prof. Yiorgos Makris).

22. "Power droop in high-performance ICs and a screening strategy". AMD Boston Design Center, Acton, USA, October 2006 (Host: Dr. Thomas Clouqueur).

23. "Power droop in high-performance ICs and a screening strategy". University of Massachusetts, Amherst, USA, September 2006 (Host: Prof. Sandip Kundu).

24. "Period of grace: A new paradigm for efficient soft error hardening". South European Test Seminar, Neustift im Stubaital, Austria, March 2006.

25. "Period of grace: A new paradigm for efficient soft error hardening". Freiburg-Innsbruck-Paderborn-Stuttgart Workshop, Freudenstadt, November 2005.

26. "Test & diagnosis in nanoscale technologies". Tokyo Metropolitan University, Tokyo, Japan, October 2005 (Host: Prof. Kazuhiko Iwasaki).

27. "Test & diagnosis in nanoscale technologies". Osaka Gakuin University, Osaka, Japan, September 2005 (Host: Prof. Kozo Kinoshita).

28. "Soft errors: The fourth dimension". Nara Institute of Science and Technology (NAIST), Nara, Japan, September 2005 (Host: Prof. Hideo Fujiwara).

29. "Test & diagnosis in nanoscale technologies". Kyushu Institute of Technology, Fukuoka, Japan, September 2005 (Host: Prof. Seiji Kajihara).

30. "Test & diagnosis in nanoscale technologies". Nara Institute of Science and Technology (NAIST), Nara, Japan, August 2005 (Host: Prof. Hideo Fujiwara).

31. "Test & diagnosis in nanoscale technologies". Annual Meeting of the Professorial Advisory Board of the German Informatics Society (GIBU), Dagstuhl, Germany, March 2005 (four of the finalists of the GI Best Dissertations 2003 Award were invited).

32. "Non-concurrent BIST for soft error detection". South European Test Seminar, St. Leonhard, Austria, March 2005.

33. "Transient fault modeling and detection in dynamic noisy environments". Freiburg-Innsbruck-Stuttgart Workshop, Innsbruck, Austria, December 2004.

34. "The pros and cons of Very-Low-Voltage testing". University of Michigan, Ann Arbor, USA, October 2004 (Host: Prof. John P. Hayes).

35. "The pros and cons of Very-Low-Voltage testing". Stanford University, USA, April 2004 (Host: Prof. Edward McCluskey).

36. "Maximally dominating faults and n-detection". Freiburg-Innsbruck-Stuttgart Workshop, Freiburg, November 2003.

37. "System-on-a-chip test: an overview and a new result". Princeton University, USA, December 2002 (Host: Prof. Niraj Jha).

38. "System-on-a-chip test: an overview and a new result". University of Wisconsin, Madison, USA, December 2002 (Host: Prof. Kewal Saluja).

39. "Maximally dominating faults and n-detection". Purdue University, West Lafayette, USA, November 2002 (Host: Prof. Irith Pomeranz).

40. "Defect-based test". Micronas GmbH, Freiburg, Germany, November 2001 (Host: Hartmut Delong).

41. "BIST for delay faults". University of Iowa, Iowa City, USA, August 1999 (Host: Prof. Sudhakar Reddy).